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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.
09/200,935	11/30/98	YANG Y	0630-0870P

002292 MMC1/0615
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EXAMINER	
JEAN PIERRE,P	
ART UNIT	**PAPER NUMBER**
2819	7

DATE MAILED: 06/15/00

Please find below and/or attached an Office communication concerning this application or proceeding.

Commissioner of Patents and Trademarks

Office Action Summary

Application No.	Applicant(s)
09/200,935	Yang
Examiner	**Group Art Unit**
Peguy JeanPierre	2819

☒ Responsive to communication(s) filed on *May 12, 2000*.

☐ This action is **FINAL**.

☐ Since this application is in condition for allowance except for formal matters, **prosecution as to the merits is closed** in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11; 453 O.G. 213.

A shortened statutory period for response to this action is set to expire *3* month(s), or thirty days, whichever is longer, from the mailing date of this communication. Failure to respond within the period for response will cause the application to become abandoned. (35 U.S.C. § 133). Extensions of time may be obtained under the provisions of 37 CFR 1.136(a).

Disposition of Claims

☒ Claim(s) *1-34* is/are pending in the application.

Of the above, claim(s) _____ is/are withdrawn from consideration.

☐ Claim(s) _____ is/are allowed.

☒ Claim(s) *1-34* is/are rejected.

☐ Claim(s) _____ is/are objected to.

☐ Claims _____ are subject to restriction or election requirement.

Application Papers

☐ See the attached Notice of Draftsperson's Patent Drawing Review, PTO-948.

☐ The drawing(s) filed on _____ is/are objected to by the Examiner.

☐ The proposed drawing correction, filed on _____ is ☐approved ☐disapproved.

☐ The specification is objected to by the Examiner.

☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. § 119

☐ Acknowledgement is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d).

☐ All ☐ Some* ☐ None of the CERTIFIED copies of the priority documents have been

☐ received.

☐ received in Application No. (Series Code/Serial Number) _____.

☐ received in this national stage application from the International Bureau (PCT Rule 17.2(a)).

*Certified copies not received: _____.

☐ Acknowledgement is made of a claim for domestic priority under 35 U.S.C. § 119(e).

Attachment(s)

☒ Notice of References Cited, PTO-892

☐ Information Disclosure Statement(s), PTO-1449, Paper No(s). _____

☐ Interview Summary, PTO-413

☐ Notice of Draftsperson's Patent Drawing Review, PTO-948

☐ Notice of Informal Patent Application, PTO-152

--- SEE OFFICE ACTION ON THE FOLLOWING PAGES ---

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. Claims 1-34 are rejected under 35 U.S.C. 103(a) as being unpatentable over Walters (USP 4,408,272) in view of Hoffert (USP 5,502,837).

With regard to claims 1-2, Walters discloses in Figure 10 a serial to parallel converter (shift register 120) (see col. 11, lines 50-55) which converts a serial data to a parallel data having a data length of 8 bits or 16 bits (see col. 12, lines 4-7). The data length is made by a length selection circuit (35) under control of the control word stored in a control register (37) connected to the serial parallel converter. With regard to claims 16-17, Walters further disclose in Figure 1 a parallel to serial converter (shift register 20) (see col. 2, lines 44-46) which converts a parallel data to a serial data having a data length of 8 bits or 16 bits (see col. 3, lines 19-21). The data length is made by a length selection circuit (35) under control of the control word stored in a control register (37) connected to the parallel to serial converter (20). The shifting of the data length parallely or serially depends on a clock/sync generator (28) connected to the converters (20, 120) via gate (30). The system of Walters further comprises two bits L1, L0, which select the length of the data to be transmitted (see col. 7, lines 38-41).

In considering claims 1-2 and 16-17, Walters does not teach the selection of the clock signal in response to the mode signal or the data length format. Hoffert discloses in column 6, lines 17-35, a clock signal (81) which synchronizes a counter (42) to generate clock outputs (73-75) at frequencies required for a 32, 16 or 8 bit mode signal, a multiplexer (41) which selects one of the output clocks (73-75) in relation to the data length format. Therefore, it would have been obvious to one having ordinary skill in the art to modify the system of Walters by selecting the clock signal based on the mode signal or the datalength to be processed for the benefit of sequentially shifting the desired length of data efficiently and accurately in a timely manner, thereby, improving system's synchronization.

In considering claims 5-15 and 20-34, Walters does not teach a first, a second, a third, and a fourth transfer units which include a first, a second, a third, and a fourth shift registers. It is readily admitted in the Prior art Figure 1 a clocking scheme (20, 30) coupled to a plurality of transfer units as illustrated in Figure 2 and includes a first and a second transfer units (TX1, TX2) having a first and a second shift registers having the same bit storage capacity. Shift registers are electronic circuits which are known in the art to store digital data, transmit the stored digital data or a portion of the stored digital data according to a particular setting or mode. It is further known in the art that the timing, the format (parallel or serial) in which the register transmit the stored digital data is function of the inputted clocking scheme. The clocking scheme generally has variable pulses, intervals, periods which vary according to the length of the data subjected to be transferred. Therefore, it would have been obvious to one having ordinary skill in the art to

modify Walters by providing the clocking scheme to the plurality of shift registers as taught by the Prior Art for the benefit of shifting a desired length of data efficiently in a timely manner.

Conclusion

3. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. Chiba et al. (USP 5,935,237) disclose data transfer apparatuses having a variable length format.

Response to Arguments

4. Applicant's arguments with respect to claims 1-34 have been considered but are moot in view of the new ground(s) of rejection.

5. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Peguy JeanPierre whose telephone number is (703) 308-1968. Any inquiry of a general nature or related to the status of this application should be directed to the Group receptionist whose telephone number is (703) 308-0956. The Group fax number is (703) 308-7722.

Peguy JeanPierre

Peguy JeanPierre

June 13, 2000